09/257,506

AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An integrated circuit for liquid crystal display characterized in that multi-port data output signals are generated with respect to a data input signal, and points of changing said data output signals with respect to a time base are set with time delays that lag one another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced.

2. (Previously Presented) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively delayed from an active edge of the clock output signal by 0.5 period, 1 period, and 1.5 period of the data input signal.

C1 Cont

3. (Previously Presented) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal.

4. (Previously Presented) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input

signal and by a delay time produced by a delay circuit added to the optional integer times as long as a half period of the data input signal.

5. (Previously Presented) A liquid crystal display characterized in that multi-port display data output signals are generated with respect to a data input signal, and points of changing said display data output signals with respect to a time base are set with time delays that lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous changes of display data output signals is reduced.

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6. (Original) A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively delayed from the active edge of the clock output signal by 0.5 period, 1 period, and 1.5 period of the clock input signal or the display data input signal.

7. (Previously Presented) A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal.

8. (Previously Presented) A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to

points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal and by a delay time produced by a delay circuit added to the integer times as long as the half period of the clock input signal or the display data input signal.

9. (Previously Presented) A driving method of a liquid crystal display characterized in that when red, green and blue color display data composed of plural bits are transferred from a display timing circuit to a TFT drive circuit for driving a TFT liquid crystal panel to display, each transfer is performed with a time delay that lags incrementally for each bit unit formed of plural bits optionally selected from each of said display data.

C1 cont

10. (Original) A driving method of a liquid crystal display according to claim 9, wherein the bit unit is formed for each of red, green and blue color display data.

11. (Original) A driving method of a liquid crystal display according to claim 9, wherein each bit unit has a part of the plural bits forming the red, green and blue color display data.

12. (Original) A driving method of a liquid crystal display according to claim 9, wherein the bit unit is transferred with a time lag of 2 nanoseconds or longer.

13. (Original) A driver of a liquid crystal display comprising: a TFT drive circuit for driving a TFT liquid crystal panel to display; a display timing control circuit for transferring red, green and blue color display data formed of plural bits to the TFT drive circuit for each bit unit formed of plural bits optionally selected from each of the color display data; and a delay unit provided in the display timing control circuit to delay the transfer timing between one bit unit and another.

Claims 14-18 (Cancelled)